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10/562,282	12/22/2005	Christianus Hermanus Leopold Weijtens	DE030223	5688
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EXAMINER				
PIZIALI, JEFFREY J				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

10/562,282

Applicant(s)WEIJTENS, CHRISTIANUS
HERMANUS LEOPOLD**Examiner**

JEFF PIZIALI

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 12, 15, 16, 18 and 19 is/are pending in the application.
- 4a) Of the above claim(s) 7-9, 16, 18 and 19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 12 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 July 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on *12 June 2009* has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings were received on *16 July 2008*. These drawings are acceptable.
4. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102 / 103

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. *Claims 1-6, 12, and 15* are rejected under 35 U.S.C. 102(b) as anticipated by ***Hebiguchi (US 6,292,237 B1)*** or, in the alternative, under 35 U.S.C. 103(a) as obvious over ***Hebiguchi (US 6,292,237 B1)*** in view of ***Reita (REITA C: "Integrated Driver Circuits for Active Matrix Liquid Crystal Displays," Vol. 14, No. 2, 1993, pages 104-114).***

Regarding claim 1, ***Hebiguchi*** discloses a display unit [e.g., *Figs. 9A*] comprising:

a display [e.g., Fig. 9A: matrix 41] including display elements [e.g., Fig. 11: pixels PX in odd columns $j-2, j, j+2$] which are combined into groups of display elements [e.g., Fig. 10: pixels PX connected to a first gate line group G1a-G480a],

a circuit arrangement [e.g., Fig. 10: first flip-flop groups 131-134A in REG1-480 of shift register 46] for controlling the display,

the circuit arrangement including switches [e.g., Fig. 10: transfer gates 131A, 133A] and inverters [e.g., Fig. 10: inverters 132A, 134A] which are connected in series to form a series arrangement [e.g., Fig. 10: a series arrangement of 480 first flip-flop groups 131-134A],

each group of the groups of display elements [e.g., Fig. 10: each pixel PX connected to a first gate line group G1a-G480a] is connected to an output of one of the inverters [e.g., Fig. 10: inverters 132A, 134A], and

at least one clock bus line [e.g., Fig. 10: two-phase clocks CK1, CK2] to supply a first clock signal [e.g., Fig. 10: first phase clock CK1] and a second clock signal [e.g., Fig. 10: second phase clock CK2], wherein

a first set of the switches [e.g., Fig. 10: first transfer gates 131A] is closed with the first clock signal [e.g., Fig. 10: first phase clock CK1] when a second set of the switches [e.g., Fig. 10: second transfer gates 133A] is opened with the second clock signal [e.g., Fig. 10: second phase clock CK2] so that

after application of a third clock signal [e.g., Fig. 10: start pulse SPA] to an input of the series arrangement,

at least one of the groups of display elements is activated, wherein

the display elements are arranged in rows [e.g., *Fig. 10: pixels PX arranged in 480 rows formed by first gate line group G1a-G480a*], and wherein

a number of connections to elements [e.g., *Fig. 10: CK1, CK2, SPA, positive bus line, and negative DC bus line -- resulting in 5 external connections*] external to the display unit for controlling the display unit is 5 or 7

(see the entire document, including Column 8, Line 53 - Column 9, Line 45).

Should it be shown that **Hebiguchi** teaches the claimed "inverter" subject matter with insufficient specificity:

Reita discloses an inverter being formed by a parallel arrangement of a p-transistor and a second n-transistor (see the entire document, including *Fig. 5(b): Page 109*).

Using **Reita's** CMOS inverter [*Fig. 5(b)*] to form **Hebiguchi's** inverters [e.g., *Fig. 10: 132A, 134A*] would also result in the number of external connections for controlling the display unit being 5 or 7.

Hebiguchi and **Reita** are analogous art, because they are from the shared inventive field of shift registers comprising inverters for driving display units.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Reita's** CMOS inverter [*Fig. 5(b)*] to form **Hebiguchi's** inverters [e.g., *Fig. 10: 132A, 134A*], so as to use a commonly known and well understood inverter circuit that results in low operational power consumption.

Regarding claim 2, **Hebiguchi** discloses a carrier on which the display elements are arranged in a display field, wherein

the at least one clock bus line extends along an edge of the display field (*see the entire document, including Figs. 9A, 9B, 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 3, **Hebiguchi** discloses the groups of display elements are each formed by a row or a column of a matrix display (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 4, **Hebiguchi** discloses each switch of the switches is formed by a first n-transistor, and

each inverter of the inverters is formed by a parallel arrangement of a p-transistor and a second n-transistor (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Reita discloses each inverter of the inverters is formed by a parallel arrangement of a p-transistor and a second n-transistor (*see the entire document, including Fig. 5(b); Page 109*).

Regarding claim 5, **Hebiguchi** discloses the groups of display elements are connected to respective outputs of the inverters of the series arrangement (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 6, **Hebiguchi** discloses the groups of display elements include sampled rows or sampled columns of a matrix display (*see the entire document, including Fig. 10; and Column 8, Line 53 - Column 9, Line 45*).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, **Hebiguchi** discloses a display unit [*e.g., Fig. 9A*] comprising:

display elements [*e.g., Fig. 11: pixels PX in odd columns $j-2, j, j+2$*];

series arrangements [*e.g., Fig. 10: 480 series arrangements of first flip-flop groups 131-134A*] between the display elements, wherein

each of the series arrangements includes a first switch [*e.g., Fig. 10: first transfer gate 131A*] capable of connection to a first inverter [*e.g., Fig. 10: first inverter 132A*] and

a second switch [*e.g., Fig. 10: second transfer gate 133A*] capable of connection to a second inverter [*e.g., Fig. 10: second inverter 134A*];

a first bus for a first clock [*e.g., Fig. 10: first phase clock CK1*] for controlling the first switch;

a second bus for a second clock [*e.g., Fig. 10: second phase clock CK2*] for controlling the second switch; wherein

the first switch and the second switch are alternately controlled by the first clock and the second clock, respectively, so that

when the first switch is opened then the second switch is closed; and

a third bus for a third clock [e.g., *Fig. 10: start pulse SPA*] for application to an input of one of the series arrangements so that

groups of the display elements are consecutively activated, wherein

the display elements are arranged in rows [e.g., *Fig. 10: pixels PX arranged in 480 rows formed by first gate line group G1a-G480a*], and wherein

a number of connections to elements [e.g., *Fig. 10: CK1, CK2, SPA, positive bus line, and negative DC bus line -- resulting in 5 external connections*] external to the display unit for controlling the display unit is 5 or 7

(see the entire document, including Column 8, Line 53 - Column 9, Line 45).

Should it be shown that **Hebiguchi** teaches the claimed "inverter" subject matter with insufficient specificity:

Reita discloses an inverter being formed by a parallel arrangement of a p-transistor and a second n-transistor (see the entire document, including *Fig. 5(b): Page 109*).

Using **Reita's** CMOS inverter [*Fig. 5(b)*] to form **Hebiguchi's** inverters [e.g., *Fig. 10: 132A, 134A*] would also result in the number of external connections for controlling the display unit being 5 or 7.

Hebiguchi and **Reita** are analogous art, because they are from the shared inventive field of shift registers comprising inverters for driving display units.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use **Reita's** CMOS inverter [Fig. 5(b)] to form **Hebiguchi's** inverters [e.g., Fig. 10: 132A, 134A], so as to use a commonly known and well understood inverter circuit that results in low operational power consumption.

Regarding claim 15, **Hebiguchi** discloses at least one of the first bus and the second bus is arranged along an edge of the display unit (see the entire document, including Figs. 9A, 9B, 10; and Column 8, Line 53 - Column 9, Line 45).

Response to Arguments

9. Applicant's arguments filed 12 June 2009 have been fully considered but they are not persuasive.

The Applicant contends, "*It is respectfully submitted that **Hebiguchi** merely discloses 6 of external connections, such as CK1, CK1, SPA, SPB shown in FIG 10 and positive and negative DC bus lines to result in 6 external connections. There is simply no disclosure or suggestion in **Hebiguchi** that the number of connections to elements external to the display unit for controlling the display unit is 5 or 7, as currently recited in independent claims 1 and 12*" (see Page 10 of the Response filed 12 June 2009). However, the examiner respectfully disagrees.

Hebiguchi discloses the number of connections to elements [e.g., Fig. 10: CK1, CK2, SPA, positive bus line, and negative DC bus line -- resulting in 5 external connections] external

to the display unit for controlling the display unit is 5 (*see the entire document, including Column 8, Line 53 - Column 9, Line 45*).

Hebiguchi mentions a second start pulse [*e.g., Fig. 10: SPB*] connection (*which the Applicant argues constitutes a 6th connection*) for feeding a second set of flip-flops [*e.g., Fig. 10: 131-134B*]. However, the second start pulse [*e.g., Fig. 10: SPB*] does not contribute to the first set of flip-flops [*e.g., Fig. 10: 131-134A*] -- and therefore does not count towards the "5 external connections" total.

Moreover, even if assuming *Hebiguchi's* circuit arrangement [*e.g., Fig. 10: first flip-flop groups 131-134A*] arguably did require all of the signals CK1, CK2, SPA, SPB, positive DC, negative DC (*i.e., six signals total*); clocks CK1 & CK2 have opposite/inverted phases.

In another embodiment, *Hebiguchi* teaches a single external signal connection [*Fig. 8: Vselect*] being divided into two opposite/inverted phases via an inverter [*Fig. 8: 120*].

Therefore, it would have been obvious to an artisan to manufacture *Hebiguchi's* circuit [*e.g., Fig. 10: 131-134A*] in a known fashion, using only one external clock connection, dividing the clock signal into two opposite/inverted phases via an inverter, and resulting in the "5 external connections," being instantly claimed.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFF PIZIALI whose telephone number is (571)272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
30 July 2009